



PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional) 59643.00238
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on _____		Application Number: 10/632,089 Filed: August 1, 2003
Signature _____		First Named Inventor: Olav Tirkkonen Art Unit: 2618
Typed or printed Name _____		Examiner: Duc M. Nguyen

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a Notice of Appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Note: No more than five (5) pages may be provided.

I am the

- Applicant/Inventor.
 assignee of record of the entire interest.
See 37 CFR 3.71. Statement under
37 CFR 3.73(b) is enclosed

Attorney or agent of record.
Registration No. 33,125

Attorney or agent acting under 37 CFR 1.34.
Reg. No. is acting under 37 CFR 1.34 _____



Signature

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Typed or printed name

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Date

December 20, 2006

NOTE: Signatures of all of the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

- *Total of _____ forms are submitted.



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Olav TIRKKONEN et al.

Art Unit: 2618

Application No.: 10/632,089

Examiner: Duc M. Nguyen

Filed: August 1, 2003

Attorney Dkt. No.: 59643.00238

For: POWER ALLOCATION IN A COMMUNICATION SYSTEM

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

December 20, 2006

Sir:

This is a Pre-Appeal Brief Request for Review from the final rejection noted in the Official Action dated June 20, 2006 (the Office Action), and maintained in an Advisory Action dated December 8, 2006, which finally rejected all of claims 1-23.

Applicants filed a Response including minor amendments on November 20, 2006. In the Advisory Action, it was indicated that upon the filing of an Appeal, the amendments of November 20, 2006, would be entered.

As will be discussed below, Applicants respectfully submit that the rejections noted in the Official Action dated June 20, 2006, contained clear error, and therefore should be withdrawn. A Notice of Allowance, therefore, is respectfully requested.

The following prior art rejections were made against the presently pending claims:

Claims 1, 18, and 23 were rejected under 35 USC 102(a) as being anticipated by *Sadjadpour* (U.S. Patent Publication No. 2001/0055332).

Claims 2-13, 19, 20, and 22 were rejected under 35 USC 102(a) as being unpatentable over *Sadjadpour*, in view of Applicants' admitted prior art shown in Figures 1 and 2 of the application (AAPA). The Office Action took the position that *Sadjadpour* disclosed all the elements of the claims, with the exception of a MIMO system. The AAPA were cited as curing deficiencies in *Sadjadpour*.

Claims 14-17, and 21 were rejected under 35 USC 103(a) as being obvious over *Sadjadpour*, in view of AAPA, and further in view of *Kim* (U.S. Patent Publication No. 2003/0128769). In making this rejection, the Office Action took the position that *Sadjadpour* disclosed all the elements of the invention except for codings and modulations that utilize system bits. The AAPA and *Kim* were cited as curing the deficiencies in *Sadjadpour*.

As will be discussed below, Applicants respectfully submit that the primary reference of *Sadjadpour*, when being alone or when combined with the secondary and tertiary references of AAPA and *Kim*, fail to disclose or suggest all the elements of the presently pending claims. This failure constitutes clear factual error, thereby requiring that the rejections be withdrawn.

In the interest of brevity, the subject matter of the presently pending claims will not be repeated here. Please refer to Applicants' Response of November 20, 2006, for a full characterization of the embodiments of the invention as recited in the claims.

Sadjadpour discloses a method and apparatus for minimizing near and cross talk due to discrete multi-tone transmission in cable binders. In other words, *Sadjadpour* is directed to a multi-tone modem that operates to minimize crosstalk over, for example, a twisted pair table. Referring to figure 4 and paragraph 27 of *Sadjadpour*, digital modulator 14 can generate N QAN signal tones, one for each channel. Each channel can handle k_i bits of data, where i is the number of the channel. A serial-to-parallel buffer 41 segments a serial stream of digital data into N frames, with each having allocated k_i bits of data, which are in turn applied to respective inputs of a multi-carrier modulator 42, which generates a QAN tune for each channel. The bit addition algorithm of *Sadjadpour* describes how an array of different bit allocation settings are ordered in ascending order so that bit allocation can be determined based on the least possible power for the maximum data rate possible or a desired data rate, as described in paragraphs [0037]-[0038]. Bits are then added and the process continued until the addition of any further bit in any of the frequency bins violates at least one predetermined constraint, such as power budget, power mask, or maximum number of bits per frame. Further, in another described embodiment of *Sadjadpour*, the method of allocating bits is modified by modifying the incremental power term by a weighting dependent on the frequency of the tone (sub-frequency). The effect of this weighting function forces the algorithm towards the lower frequencies, which according to the disclosure, has the effect or goal of reducing the near end cross talk (NEXT) power. The Office Action took the position that *Sadjadpour* disclosed, at paragraphs 43-46, modulation circuitry having a plurality of modulation alphabets providing a set of bit loading sequences, circuitry configured to determine power allocation for at least one bit loading sequence based on minimizing an error rate, and circuitry configured to select a bit loading sequence with a lowest error rate, as recited in Applicants' claim 1, and similar to that recited in other independent claims. However, Applicants respectfully submit that no such disclosure exists in *Sadjadpour*. Paragraphs 43-46 of *Sadjadpour* are directed to Figure 6 thereof, and they are directed to blocks 61-68 representing various objective functions that can be

identified from various algorithms. Function 64 is directed to representing minimization of an arbitrary function of total power and maximization of total data rate. Block 61 of *Sadjadpour* illustrates functions which can apply joined minimization of the cross talk and maximization of the total data rate. A further discussion of this aspect of *Sadjadpour* can be found in paragraphs 39-42 thereof. However, Applicants respectfully submit that there is simply no disclosure nor suggestion in *Sadjadpour* of any elements which could be comparable to the circuitry as recited in the presently pending claims, wherein a power allocation is determined for at least one bit loading sequence based on minimizing an error rate. As discussed above, and as discussed in Applicants' previous responses, the present invention is directed to a device which contains circuitry and which can perform a step of selecting a bit loading sequence based on a lowest error rate.

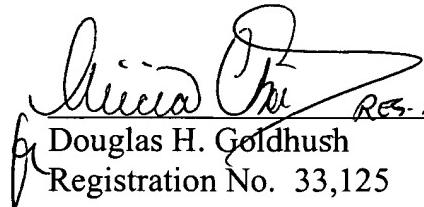
Applicants respectfully submit that the failure of *Sadjadpour* to disclose or suggest such circuitry, or any steps which select a bit loading sequence with a lowest error rate, is a clear error which requires that the outstanding rejections be withdrawn.

Applicants respectfully submit that the AAPA and/or *Kim* fails to cure the deficiencies which exist in *Sadjadpour*. The "related art" sections of the application do discuss the fact that (multiple-input multiple-output) systems can distribute a user signal between transmitting antenna. The description of related art also discusses that a result of the system is that overall quality of transmission can be improved. However, neither *Sadjadpour* nor the AAPA utilizes the circuitry which is recited in any of claims 1-17, and 19, or any steps as recited in the methods of claims 18, 20, or 21, or the means as recited in claims 22 and 23, wherein power weighting to a corresponding logical channel is allocated for minimizing a bit error rate of an identified bit loading sequence, and wherein a minimum bit error rate is selected.

Conclusion

As discussed above, it is respectfully and strongly submitted that there is clear factual error with regard to the various rejections of claims 1-23. These claims each recited elements which are neither disclosed nor suggested in any combination of *Sadjadpour*, AAPA, and/or *Kim*. It is therefore respectfully requested that the rejections of these claims be reversed, and that this application passed to issue.

Respectfully submitted,



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Enclosures: PTO/SB/33 Form
Notice of Appeal
Check No. 15575